

SCiswitchdrive11\_i

#### **Preliminary Information**

#### HIGHLIGHTS

- -For driving up to 1200V IGBT or MOSFET
- -2 control modes
- -Trigger-schmidt logic inhibition input
- for high noise inmunity
- -Wide spread of supply voltage: 7-20V
- -Configurable rise and fall times
- -Electrical isolation of 3000Vac
- -Easy to use

# SCISwitch<sup>Drive</sup>11

IGBT/MOSFET gate driver for SSR design



Photo non-contractual

#### TYPICAL APPLICATIONS



**SCi**Switch<sup>Drive</sup>**11** is a MOSFET & IGBT firing board which implements the usual gate driver functions. It has been designed for making DC solid state relays (thanks to the connection of a power MOSFET in the output). It provides a galvanic isolation up to  $3000V_{AC}$  between input and output.

**SCi***Switch*<sup>Drive</sup>**11** is capable of generate enough output peak current to switch the MOSFET in a few microseconds, it allows firing the MOSFET in parallel configuration.

The switching time of the MOSFET can be set by changing inner resistors (R1 & R2).

**SCi***Switch*<sup>Drive</sup>**11** turns on the MOSFET at a constant voltage of 13V, regardless of the supply voltage level. For easier using, the triggering can be done by switching the power supply of the board (supply mode control), as well, with logic inhibition signal and permanent input supplied (inhibition mode control). Includes a LED that monitors the MOSFET status.

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#### **ELECTRICAL CHARACTERISTICS**

Description	symbol	notes/test conditions	Min	Тур	Max	Units
Supply voltage	V <sub>cc</sub>		7	12	20	V
Current consumption	lcc				120	mA
Inhibition input high logic state	$V_{INH_{HIGH}}$				5	V
Inhibition input low logic state	$V_{\text{INH}_{\text{LOW}}}$		0			V
Inhibition high-going treshold voltage	V <sub>INH_H&gt;L</sub>			3,3		V
Inhibition low-going treshold voltage	V <sub>INH_L-&gt;H</sub>			1,8		V
Gate-source output voltage	V <sub>GS</sub>		12,2	13	13,5	V
Gate-source voltage ripple					5	%
Output Peak current	I <sub>PEAK</sub>				250	mA
Resistor R1 value	R1	note 1	50		470	Ω
Resistor R2 value	R2	note 1	2,2		100	kΩ
Input-to-output isolation	V <sub>ISO</sub>	1 min @ 50Hz	3000			$KV_{AC}$
Supply-to-output delay	t <sub>dON_vcc</sub>	supply mode control		6		μs
Supply-to-output delay	$t_{dOFF_vcc}$	supply mode control		10		μs
Inhibition-to-output delay	t <sub>dON_INH</sub>	inhibition mode control		1		μs
Inhibition-to-output delay	t <sub>dOFF_INH</sub>	inhibition mode control		1		μs
Output voltage rise time	t <sub>rise</sub>	10% to 90% V <sub>GS</sub> note 2				μs
Output voltage fall time	t <sub>fall</sub>	10% to 90% V <sub>GS</sub> note 2				μs

#### **TRIGGER MODE**

There are 2 ways to switch the output voltage: the supply mode control and the inhibition mode control. In the supply mode control, only 1 signal (VCC) is required to control the entire SSR. This signal supplies the circuit board and turns the output to high state (13V) while the voltage level (VCC) is over 7V, otherwise the output remains to low state (0V). In this mode the INH input must remain no connected. In the inhibition mode control, a permanent supply is required (VCC>7V) and the INH signal (TTL compatible and low sinked current) controls the output. In this mode some SSRs could be controlled directly by digital master system. In each mode the output state is monitorized by the on state LED.

Supply	mode	control

Inhibition mode control

VCC	INH	LED	V <sub>GS</sub>
L	N.C.	OFF	L
Н	N.C.	ON	н
Н	L	OFF	L
Н	Н	ON	Н

**note 1**: Allways respecting the proportion: R2>20xR1 in order to mantain  $V_{GS}$  level and ripple into his margins. **note 2**: rise time and fall time depens on the value of the resistors R1 and R2





#### **RISE & FALL TIME CONFIGURATION**

In order to obtain softer or harder switching of the outer MOSFET, rise and fall times can be set by changing the value of the resistors R1 and R2. The equivalent gate capacitance of the outer MOSFET ( $C_G$ ) must be known. An aproximated way to obtain the times is:

 $t_{rise}[\mu s] \approx 2 \cdot R1[\Omega] \cdot (C_G[uF] + 0.22)$  $t_{fall}[\mu s] \approx 2 \cdot R2[\Omega] \cdot (C_G[uF] + 0.22)$ 

#### FIRING MOSFET IN PARALEL CONFIGURATION

**SCi**Switch<sup>Drive</sup>**11** hasn't limitation by MOSFET gate charge. It allows to connect more than one MOSFET at the **SCi**Switch<sup>Drive</sup>**11** output in order to get a larger drain current SSR. In that case  $C_{g}$  for rise and fall time calculations must be the sum of each individual gate capacitance.

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#### **MECHANICAL DIMENSIONS & PINOUT**







All dimensions are in milimeters





**MECHANICAL DIMENSIONS & PINOUT** 

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