## Adaptation board for SCiCoreDrive22

### DEFAULT VALUES (board configuration)

- Half-bridge mode (Direct mode optional)
- 4 µs dead time between channels (configurable)
- Gate resistors not mounted
- 0-5 V input PWM logic levels (0-15 V configurable)
- 0-5 V fault output


*Non-contractual image*

**SCiCoreLink62** is a printed circuit board specially designed for interfacing and work with the 2-channel IGBT driver module **SCiCoreDrive22.**
For further information and technical specifications about the behaviour of the entire driver board, timming and electrical characteristics, please refer to **SCiCoreDrive22** datasheet.
Gate resistors are not included (by default), can be mounted under order.
Other configurations than the default one can be supplied under order, please contact with us.

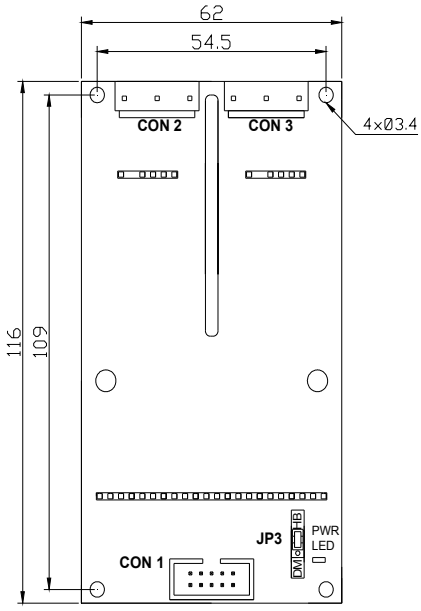
### ELECTRICAL CHARACTERISTICS

| Description | Symbol | Notes / Test conditions | Min | Typ | Max | units |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | 14 | 15 | 16 | $V_{DC}$ |
| PWM High state input voltage 0-5V | $V_{PWM\_H}$ | *JP1 & JP2 connected (1)* | 3.5 | 5 | 5 | V |
| PWM Low state input voltage 0-5V | $V_{PWM\_L}$ | | 0 | 1.5 | 1.5 | V |
| PWM High state input voltage 0-15V | $V_{PWM\_H15}$ | *JP1 & JP2 unconnected (1)* | 11 | | 15 | V |
| PWM Low state input voltage 0-15V | $V_{PWM\_L15}$ | | 0 | | 4 | V |
| Reset High state input voltage | $V_{RESET\_H}$ | | 2 | | 5 | V |
| Reset Low state input voltage | $V_{RESET\_L}$ | | 0 | | 0.8 | V |
| Fault High state output voltage | $V_{FAULT\_H}$ | | | | 5 | V |
| Fault Low state output voltage | $V_{FAULT\_L}$ | *indicates fault condition* | 0 | | 0.4 | V |

*(1): JP1 and JP2 jumpers are located at SCiCoreDrive22, not at SCiCoreLink62*

### MECHANICAL DIMENSIONS

| Description | |
|---|---|
| PCA general dimensions | 62 x 116 x 15 mm |
| Fixation holes | Drill holes 4x Ø 3.4 mm |
| Weight | 35 gr. aprox. |




*All dimensions in mm*

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## PINOUT

| CON1 | Designation | Description |
|---|---|---|
| 1 | IN2 | Input logic signal switching channel 2 |
| 2 | GND | Ground terminal for supply and logic signals |
| 3 | GND | Ground terminal for supply and logic signals |
| 4 | RESET | Reset input signal (low state) |
| 5 | GND | Ground terminal for supply and logic signals |
| 6 | VCC | +15 $V_{DC}$ for supply voltage |
| 7 | FAULT | Fault output signal |
| 8 | VCC | +15 $V_{DC}$ for supply voltage |
| 9 | VCC | +15 $V_{DC}$ for supply voltage |
| 10 | IN1 | Input logic signal switching channel 1 |

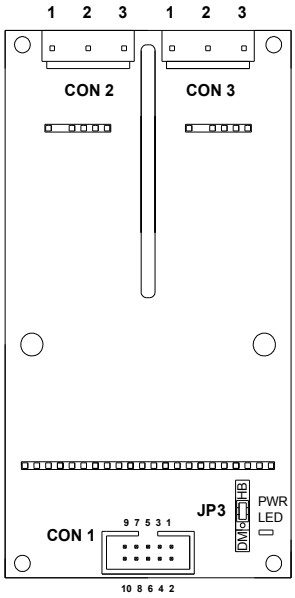
| JUMPERS | |
|---|---|
| JP1 (*) | both connected: 5 V logic level |
| JP2 (*) | both unconnected: 15 V logic level |
| JP3 | up connected: Half bridge mode<br>down connected: Direct mode |

*(*) jumpers on SCiCoreDrive22*

| CON2 | Designation | Description |
|---|---|---|
| 1 | $COLLECTOR_{CH1}$ | IGBT channel 1 collector desaturation sensing |
| 2 | $GATE_{CH1}$ | IGBT channel 1 gate signal |
| 3 | $EMITTER_{CH1}$ | IGBT channel 1 emitter signal |

| CON3 | Designation | Description |
|---|---|---|
| 1 | $COLLECTOR_{CH2}$ | IGBT channel 2 collector desaturation sensing |
| 2 | $GATE_{CH2}$ | IGBT channel 2 gate signal |
| 3 | $EMITTER_{CH2}$ | IGBT channel 2 emitter signal |

**Connector types:**
CON1 : C-Grid 70246 Series, 70246-1004, Molex. 10 pos.
CON2 & CON3: VH series, B5P-VH, JST 3 pos , 7.92 mm pitch.
Recommended matching receptacle: VHR-5N, and crimping pins: BVH-21T-P1 both from JST.



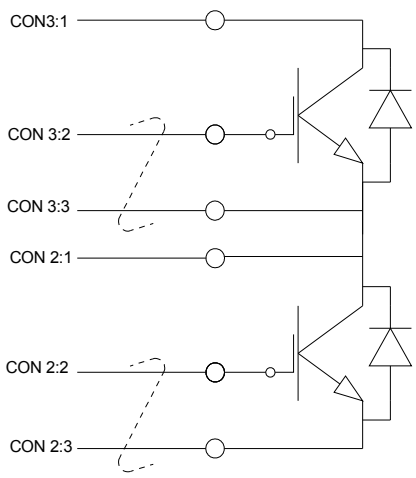




*figure 1: Example of connection.*

**- Mounting considerations:**
Cables between PCB and IGBT must be as short as possible.
Gate and emitter connections should be shielded or twisted pair.

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## GATE RESISTORS

By default the board does not include any gate resistor installed. User must solder on its designated resistors pads the required resistance. For each channel there are available 3 resistor spaces for $R_{G\ ON}$ and for $R_{G\ OFF}$. The available pads on PCB are suitable for 1206 SMD resistors.

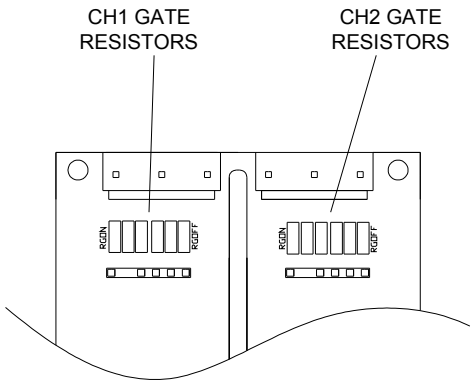


*figure 2: Detail of gate resistor pads.*

## DEAD TIME CAPACITORS

By default SCiCoreLink62 includes the dead time capacitors needed for a 4 µs between channels. Please refer to SCiCoreDrive22 datasheet if you want to change the default dead time and calculate its necessary capacitance.
The available pads on PCB are suitable for 1206 SMD capacitors. It is highly recommended a good value matching between channels of dead time capacities.

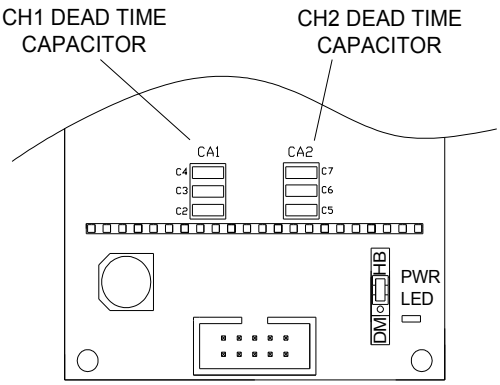


*figure 3: Detail of dead time capacitor pads.*

## FAULT OUTPUT SIGNAL

By default SCiCoreLink62 ties together both O.C. (ORing) output faults from SCiCoreDrive22 and internally connnects a pull-up resistance 3.3 kΩ to the line in order to provide the logic fault signal of 0-5 V on CON1.

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